REMARKS

The present amendment is in response to the Office Action, dated March 22, 2003, where the Examiner has rejected claims 1-16, 32-36 and 61-120. By the present amendment, claims 106-112 have been canceled, and claim 32, 83-91, 113 and 118 have been amended. After the present amendment, claims 1-16, 32-36, 61-105 and 113-120 are pending in the application. Reconsideration and allowance of pending claims 1-16, 32-36, 61-105 and 113-120 in view of the amendments and the following remarks are respectfully requested.

A. Objection to the Specification

The Examiner has objected to the abstract for including the word "disclosed". By the present amendment, applicants have amended the abstract to replace the word "disclosed" with the word --provided--. Applicants respectfully submit that the Examiner's objection has been overcome.

B. Objection to Claims 32-36

The Examiner has objected to claims 32-36. In response, applicants have amended claim 32 to replace "an analog codec" with --the analog codec-- in two places, and have amended claim 32 to replace "an ATM interface" with --the ATM interface-- in two places. Accordingly, applicants respectfully submit that the Examiner's objection has been overcome.

C. Rejection of Claims 87, 88, 106-112 and 113-120 under 35 U.S.C. § 112, ¶ 1

The Examiner has rejected claims 87, 88, 106-112 and 113-120 under 35 U.S.C. § 112, ¶ 1, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner has rejected claim 87 for stating that the "system" is incorporated within a North Bridge and/or a South Bridge chipset, and rejected claim 88 for stating that the "system" is incorporated within a motherboard for a computer system. Applicants have amended claims 87 and 88 to replace the word "system" with the words --digital controller section--, and respectfully submit that the above amendment is supported by the specification.

The Examiner has rejected claims 106-112. Applicants respectfully disagree; however, in order to expedite the prosecution of the present application, applicants have canceled claims 106-112 and respectfully submit that the Examiner's rejection has been rendered moot.

The Examiner has rejected claims 113-120, because the preamble of claim 113 states: "A method of communicating data over a data link connecting a first integrated circuit located on a computer motherboard and a second integrated circuit located on the computer motherboard". Applicants have amended claim 113 to replace the words "a computer motherboard" with the words --a first circuit board--, and the words "the computer motherboard" with the words --the second circuit board--, and respectfully submit that the above amendment is supported by the specification.

Accordingly, applicants respectfully submit that the Examiner's rejection of claims 87, 88, 106-112 and 113-120 under 35 U.S.C. § 112, ¶ 1, has been overcome.

D. Rejection of Claims 32-36 and 83-91 under 35 U.S.C. § 112, ¶ 2

The Examiner has rejected claims 32-36 and 83-91 under 35 U.S.C. § 112, ¶ 2. The Examiner has rejected claim 32 for reciting the limitation "bit clock", without sufficient antecedent basis. By the present amendment, applicants have amended claim 32 to replace "bit

clock" with "clock signal", and respectfully submit that the Examiner's rejection of claims 32-36 has been overcome.

Further, the Examiner states that, in claims 83-91, essential structural cooperative relationships have been omitted. By the present amendment, applicants have amended claim 83-91. More specifically, claim 83 has been amended to recite "a digital communications link comprising: (a) a plurality of receive signal lines for communicating data received by the analog section from a remote xDSL modem to the digital controller; (b) a plurality of transmit signal lines communicating data received by the analog section from the digital controller to the remote xDSL modem; (c) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal to clock transfers between the analog section and the digital controller". Applicants respectfully submit that claims 83-91, as amended, show the relationships of the digital controller, the analog section, the plurality of receive signal lines, the plurality of transmit signal lines and the bit clock signal line.

Accordingly, applicants respectfully submit that the Examiner's rejection of claims 32-36 and 83-91 under 35 U.S.C. § 112, ¶ 2, has been overcome.

E. Rejection of Claims 1-16, 32-36 and 61-66 under the Judicially Created Doctrine of Obviousness-Type Double Patenting

The Examiner has rejected claims 1-16, 32-36 and 61-66 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16, 32-36 and 32-36 of U.S. Patent No. 6,345,072, respectively.

Along with the present amendment, applicants have submitted a terminal disclaimer to overcome the Examiner's rejection under the judicially created doctrine of obviousness-type double patenting with respect to claims 1-16 and 32-36 of U.S. Patent No. 6,345,072. Applicants

respectfully submit that the enclosed terminal disclaimer overcomes the Examiner's rejection of claims 1-16, 32-36 and 61-66 under the judicially created doctrine of obviousness-type double patenting.

F. **Rejection of Claims 1, 3-12 and 16 under 35 U.S.C. § 103(a)**

The Examiner has rejected claims 1, 3-12 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Bingham et al. (USPN 5,680,394) (hereinafter "Bingham") in view of Grube et al. (USPN 5,606,577) (hereinafter "Grube"). Applicants respectfully disagree.

The Examiner rejects claim 1 by stating that the digital controller and the analog codec of claim 1 are "broadly interpreted" to be receiving/transmitting xDSL data as in the central unit of Bingham and the remote units of Bingham. Applicants respectfully submit that the Examiner's "broad interoperation" is unfounded and ignores the limitations of claim 1. First, each of the central unit and the remote units of Bingham is a standalone DSL modem, whereas neither the digital controller of claim 1 nor the analog codec of claim 1, by itself, can be said to be a DSL modem. In fact, only the combination of the digital controller of claim 1 and the analog codec of claim 1 forms a DSL modem. Bingham fails to disclose, teach or suggest a method of implementing a digital link for use within either the central unit or the remote units. Second, the Examiner's "broad interpretation" ignores the words "digital" and "analog". The Examiner should note that the data communication between the digital controller of claim 1 and the analog codec of claim 1 is performed via a "digital" communication link. Whereas the communication between the central unit and remote units of Bingham is performed via PSTN telephone lines in modulated analog form. Accordingly, the Examiner's "broad interpretation" ignores key limitations of claim 1.

Third, and more importantly, applicants respectfully submit that Bingham and Grube fail to disclose, teach or suggest "providing a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal, which bit clock signal is generated by scaling a separate clock signal useable by the xDSL modem, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols". It should be noted that the digital link is made up of various separate signal lines, where, in sharp contrast, Bingham describes communication via a telephone line, and neither Bingham nor Grube discloses a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal. Further, Grube simply states what is already known about DSL, which is that clock rate can be variable based on the data rate, but neither Bingham nor Grube discloses, teaches or suggests that a DSL modem is broken into digital and analog portions, and that a separate clock signal carries a bit clock signal between the digital and analog portions, and which bit clock signal is generated by scaling a separate clock signal, such as the Master Clock from the host, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

Accordingly, applicants respectfully submit that claim 1 and its dependent claims 3-12 and 16 should be allowed.

G. Rejection of Claims 13-15 under 35 U.S.C. § 103(a)

The Examiner has rejected claims 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Bingham in view of Grube and further In view of Suzuki (USPN 6,529,479) (hereinafter "Suzuki"). Applicants respectfully disagree.

Applicants respectfully submit that claims 13-15 depend from claim 1 and should be allowed at least for the same reasons stated above in conjunction with patentability of claim 1.

H. Rejection of Claims 32, 33, 35 and 36 under 35 U.S.C. § 103(a)

The Examiner has rejected claims 32, 33, 35 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Bingham in view of Grube and further in view of Suzuki. Applicants respectfully disagree.

Applicants respectfully submit that claim 32 should be allowed at least for reasons similar to the first and second reasons stated above in conjunction with patentability of claim 1. Further, the cited references fail to disclose, teach or suggest "wherein said clock signal further can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link" having a plurality of receive signal lines, a plurality of transmit signal lines, and a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with both the analog codec and the ATM interface. As stated above, the cited references do not show a digital link between an analog portion and a digital portion, where the digital link includes a plurality of separate signals lines for receiving, transmitting and clocking. Grube simply states what is already known about DSL, which is that clock rate can be variable based on the data rate, but neither Bingham nor Grube discloses, teaches or suggests that a DSL modem is broken into digital and analog portions, and that the clock signal between the digital and analog portions can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link.

Accordingly, applicants respectfully submit that claim 32 and its dependent claims 33, 35 and 36 should be allowed.

I. Rejection of Claim 34 under 35 U.S.C. § 103(a)

The Examiner has rejected claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Bingham in view of Grube and Suzuki, and further in view of the admitted prior art. Applicants respectfully disagree.

Applicants respectfully submit that claim 34 depends from claim 32 and should be allowed at least for the same reasons stated above in conjunction with patentability of claim 32.

J. Rejection of Claims 67-69, 71-78, 80, 82-85, 92-98 and 99-105 under 35 U.S.C. § 103(a)

The Examiner has rejected claims 67-69, 71-78, 80, 82-85, 92-98 and 99-105 under 35 U.S.C. § 103(a) as being unpatentable over Bingham in view of Grube. Applicants respectfully disagree.

Applicants respectfully submit that claims 67-69, 71-78, 80, 82-85, 92-98 and 99-105 should be at least for the same reasons stated above in conjunction with patentability of claim 32. Further, claims 92-98 and 99-105 should be allowed, because the cited references fail to disclose, teach or suggest "generating a separate frame signal for indicating a boundary for a variable sized data frame transmitting the data between the digital controller and the analog CODEC", as recited in independent claim 92, or "a frame clock signal line for carrying a frame clock signal adapted for clocking a variable sized data frame in accordance with the bus protocol, said variable sized data frame having a size based on a number of active channels in the plurality of separate data channels and/or a desired data rate", as recited in independent claim 99.

K. Conclusion

For all the foregoing reasons, an early allowance of claims 1-16, 32-36, 61-105 and 113-120 pending in the present application is respectfully requested. Moreover, applicants direct the Examiner's attention to the Revocation and Power of Attorney, filed concurrently (a copy of which is hereby enclosed), which conveys power of attorney to the undersigned attorneys. Accordingly, applicants respectfully request that all subsequent communications be directed to:

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Tel: (949) 784-4600
Fax: (949) 784-4601

The Examiner is invited to contact the undersigned for any questions.

Respectfully Submitted;
FARJAMI & FARJAMI LLP


10/13/03

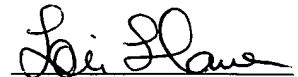
Michael Farjami, Esq.
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Tel: (949) 784-4600
Fax: (949) 784-4601

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service "First Class Mail Post Office to addressee" Service under 37 C.F.R. Sec. 1.10 addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on 10/13/03.

Lori Llave
Name


Signature